

ADICHUNCHANAGIRI UNIVERSITY
BGS INSTITUTE OF TECHNOLOGY, BG Nagara-571448
Department of Electronics & Communication Engineering

III SEMESTER TIME TABLE FOR THE YEAR 2023-24 (ODD SEMESTER)

Class Teacher: Mrs. Srividya C N

Section: C

Class Room: TB-107

| Days | 9.00 AM to 9.55 AM | 9.55 AM to 10.50 AM | T E A B R E A K | 11.00 AM to 11.55 AM | 11.55 AM to 12.50 PM | L U N C H B R E A K | 1.45 PM to 2.30 PM | 2.30 PM to 3.15 PM | 3.15 PM to 4.00 PM | |
|-----------|--------------------------|---------------------------|--|----------------------------|----------------------------|--|--------------------------|----------------------------|--------------------------|--|
| Monday | 22 MAT 31 | 22 EC 34 | | | 22 EC 35 | | 22 EC 32 | Value added Course | | |
| Tuesday | 22 EC 32 | 22 EC 34 | | | 22 EC 33 | | 22 MAT 31 | Library Hours | | |
| Wednesday | 22 EC 33 | 22 EC 32 | | | 22 EC 35 | | 22 EC 34 | AEC Lab (C1) / DS Lab (C2) | | |
| Thursday | 22 EC 34 | 22 EC 32 | | | 22 EC 33 | | 22 EC 35 | AEC Lab (C2) / DS Lab (C3) | | |
| Friday | 22 MAT 31 | 22 EC 35 | | | AEC Lab (C3) / DS Lab (C1) | | Mentoring | | | |
| Saturday | 22 EC 35 | 22 EC 33 | | | 22 MAT 31 | | 22 EC 34 | | | |

Subject Code

22MAT31
 22EC32
 22EC33
 22EC34
 22EC35
 22ECL36
 22ECL37
 22AEC 38
 22 UHV39

Subject Name

Engineering Mathematics –III
 Analog Electronics Circuits
 Digital system design using Verilog
 Network Analysis
 Signals and Systems
 Analog Electronics Circuits Lab
 Digital system design using Verilog Lab
 Soft Skill Development-I
 Sports

Staff Name

Mrs. Dhakshayini G
 Mr. Deepak R
 Mrs. Srividya C N
 Mr. Mohan Kumar K S
 Mrs. Lakshmi D L
 Mr. Mohan Kumar K S / Mr. Ravikiran H N
 Mrs. Nethravathi H M
 Ms. Bharathi R