|| Jai Sri Gurudev ||

BGS Institute of Technology

BG Nagara - 571448

Department of Electronics and Communication Engineering

Academic Year 2019-20 (Odd Semester) Master Time Table

3rd A

Days	I	II	III	IV		V	VI	VII
M	36	33	34	31	LUNCH BREAK	32	HR	
T	32	34	31	35		Lab		
W	35	Lab				36	31	33
T	36	33	34	35		36	31	32
F	34	33	35	32		Lab		
S	32	34	35	36		36	33	

18 MAT 31	Engg. Mathematics-III	Swetha H N
18 EC 32	Analog Electronics	Ramya K
18 EC 33	Computer Organization & Architecture	Balaji B S
18 EC 34	Digital Electronics	Srividya C N
18 EC 35	Network Analysis	Dr. M B Anandaraju
18 EC 36	Engineering Electromagnetics	Mohan Kumar K S
18 ECL 37	Analog Electronics Lab	Dr. M B Anandaraju/Ramya K
18 ECL 38	Digital Electronics Lab	Priyanka R /kavitha B C

3rd B

Days	I	II	III	IV		V	VI	VII
M	34	32	36	31	LUNCH BREAK	Lab		
T	35	36	32	34		33	HR	
W	31	33	35	32		Lab		
T	34	35	33	31		Lab		
F	36	32	31	34		35	33	36
S	36	36	32	35		34	36	

18 MAT 31	Engg. Mathematics-III	Parashivamurthy H L
18 EC 32	Analog Electronics	Ramya K
18 EC 33	Computer Organization & Architecture	Balaji B S
18 EC 34	Digital Electronics	Srividya C N
18 EC 35	Network Analysis	Puneeth Kumar G B
18 EC 36	Engineering Electromagnetics	Mohan Kumar K S
18 ECL 37	Analog Electronics Lab	Puneeth Kumar G B
18 ECL 38	Digital Electronics Lab	Kavitha B C/Hamsashree M K

5th A

Days	I	II	III	IV		V	VI	VII
M	54	53	52	562	LUNCH BREAK	Lab		
T	HR		553	52		53	51	54
W	562	Lab				54	51	553
T	53	52	51	553		Lab		
F	51	52	53	54		562	553	562
S	51	53	54	553		562	52	

17 ES 51	Management and Entrepreneurship	Krupesh
17 EC 52	Digital Signal Processing	Prabhavathi K
17 EC 53	Verilog HDL	Manoj Kumar S B
17 EC 54	Information Theory & Coding	Jayanth Dwijesh H P
17 EC 553	Operating System	Priyanka R
17 EC 562	Oops Using C++	Shwetha S N
17 ECL 57	DSP Lab	Jayanth Dwijesh HP/Lakshmi DL
17 ECL 58	HDL Lab	Manoj Kumar S B/Rashmi S

5th B

Days	I	II	III	IV		V	VI	VII
M	HR		54	53	LUNCH BREAK	52	553	51
T	562	51	53	54		Lab		
W	553	51	52	562		Lab		
T	54	553	53	562		51	52	562
F	53	54	553	52		Lab		
S	553	52	562	51		54	53	

17 ES 51	Management and Entrepreneurship	Krupesh
17 EC 52	Digital Signal Processing	Prabhavathi K
17 EC 53	Verilog HDL	Manoj Kumar S B
17 EC 54	Information Theory & Coding	Jayanth Dwijesh H P
17 EC 553	Operating System	Priyanka R
17 EC 562	Oops Using C++	Shwetha S N
17 ECL 57	DSP Lab	Prabhavathi K/Lakshmi D L
17 ECL 58	HDL Lab	Srividya C N

7th A									15 EC71	Microwave and Antennas	Nandini S
Days	**I**	**II**	**III**	**IV**		**V**	**VI**	**VII**	15 EC 72	Digital Image Processing	Dr. Naveen B
M	752	72	71	743		Lab			15 EC 73	Power Electronics	Kavitha B C
T	71	Lab				73	752	743	15 EC 743	Real Time Systems	Hamsashree M K
W	73	752	72	71		Project Work			15 EC 752	IoT & Wireless Sensor Networks	Nischitha S
T	743	73	72	71		Lab			15 ECL 76	Advanced Communication Lab	Nischitha S/Simha D K L N
F	743	752	72	73		Project Work			15 ECL 77	VLSI Lab	Balaji B S/ Hamsashree M K
S	Project Work					Project Work			15 ECL 78	Project Work Phase–I + Project Seminar	Jayanth Dwijesh H P/ Manoj Kumar S B/ Dr. K N Muralidhar

7th B									15 EC71	Microwave and Antennas	Nandini S
Days	**I**	**II**	**III**	**IV**		**V**	**VI**	**VII**	15 EC 72	Digital Image Processing	Dr. Naveen B
M	71	73	752	72		Project Work			15 EC 73	Power Electronics	Kavitha B C
T	73	743	71	72		Lab			15 EC 743	Real Time Systems	Bharathi R
W	72	743	73	752		Lab			15 EC 752	IoT & Wireless Sensor Networks	Nischitha S
T	752	71	743	73		Project Work			15 ECL 76	Advanced Communication Lab	Nandini S/Simha D K L N
F	72	71	743	752		Lab			15 ECL 77	VLSI Lab	Dr. Naveen B/ Dr. Naveen K B/ Rashmi S
S	Project Work					Project Work			15 ECL 78	Project Phase–I + Project Seminar	Jayanth Dwijesh H P/ Manoj Kumar S B/Dr. K N Muralidhar

Signature of HOD